

Press Release

Northwest Logic and Avery Design Systems Successfully Team on PCI Express 3.0 Solutions

ANDOVER, MA., August 8, 2011 – Northwest Logic Inc., a leader in high-performance digital IP Cores, and Avery Design Systems, a leader in Verification IP (VIP) solutions, today announced Northwest Logic's Espresso 3.0 solutions for PCI Express® (PCIe®) for Endpoint, Root Complex, and Switch have been fully verified and deployed to customers based on Avery's PCI-Xactor verification models and compliance testsuites.

"We use Avery's PCI-Xactor Verification IP to comprehensively verify our PCI Express products.," said Brian Daellenbach, president of Northwest Logic. "Avery's VIP models and compliance testsuites have been proven to provide the broad range of testing needed to fully verify PCI Express operation. In addition, Avery's support has been technically outstanding and very timely. Avery is more than a vendor to us, they are a key partner who supports us and our customer's PCI Express verification needs. We recommend Avery to all our customers for robust SoC verification."

Avery's [PCI-Xactor](#) is a complete functional verification solution for PCI Express 3.0/2.1/1.1 including feature rich models that work in any verification languages including SystemVerilog OVM and VMM methodologies, comprehensive protocol checking, functional coverage monitoring, and dedicated core and chip-level compliance test suites for Root Complex, Endpoint, SR-IOV Endpoint, Switch, and PHY designs.

"Starting a design with an IP Core that has been fully verified enables customers to achieve the shortest possible design cycles and achieve first time silicon success. Northwest Logic provides high-performance, silicon-proven complete solutions for chip designs that enable just that." said Chris Browy, Vice President of Avery Design Systems. "Our partnership with Northwest Logic has proven the exceptional quality and integrity of the IPs that is being produced by Northwest Logic."

Northwest Logic provides a complete PCI Express Solution. This solution includes Northwest Logic's high-performance, easy-to-use, silicon-proven [Espresso 3.0/2.1/1.1 Cores](#) for PCI Express, DMA Back-End Core which provides high-performance scatter-gather DMA engines, Drivers (Linux & Windows) and Application software. For a complete system design Northwest Logic optionally provides its high-performance DDR3/DDR2/DDR SDRAM Controller Cores and add-on cores (AXI/AHB, Multi-Port, Reorder,etc.). These solutions are available separately or as a single, fully integrated solution.

About Avery Design Systems

Founded in 1999, Avery Design Systems, Inc. enables system and SOC design teams to achieve dramatic functional verification productivity improvements through Insight formal analysis for improved functional verification and DFT closure, robust core-through-chip-level [Verification IP](#) for PCI Express, USB, xHCI, UAS/BOT, AXI3/4, and AHB standards, and scalable distributed parallel logic simulation. The company is a member of the Synopsys SystemVerilog and VMM Catalyst Programs, Mentor Graphics Modelsim Value Added Partnership (VAP) program, and has established numerous Avery Design VIP partner program affiliations with leading IP suppliers. More information about the company may be found at www.avery-design.com.

About Northwest Logic

Northwest Logic, founded in 1995 and located in Beaverton, Oregon, provides high-performance, silicon-proven, easy-to-use IP cores including high-performance [Expresso Solution](#) (PCI Express 3.0, 2.1 and 1.1 cores and drivers), [Memory Interface Solution](#) (DDR3, DDR2, DDR, Mobile DDR SDRAM; RLD RAM II), and [MIPI Solution](#) (CSI-2, DSI). These solutions support a full range of platforms including ASICs, Structured ASICs and FPGAs. For additional information, visit www.nwlogic.com or contact info@nwlogic.com.

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