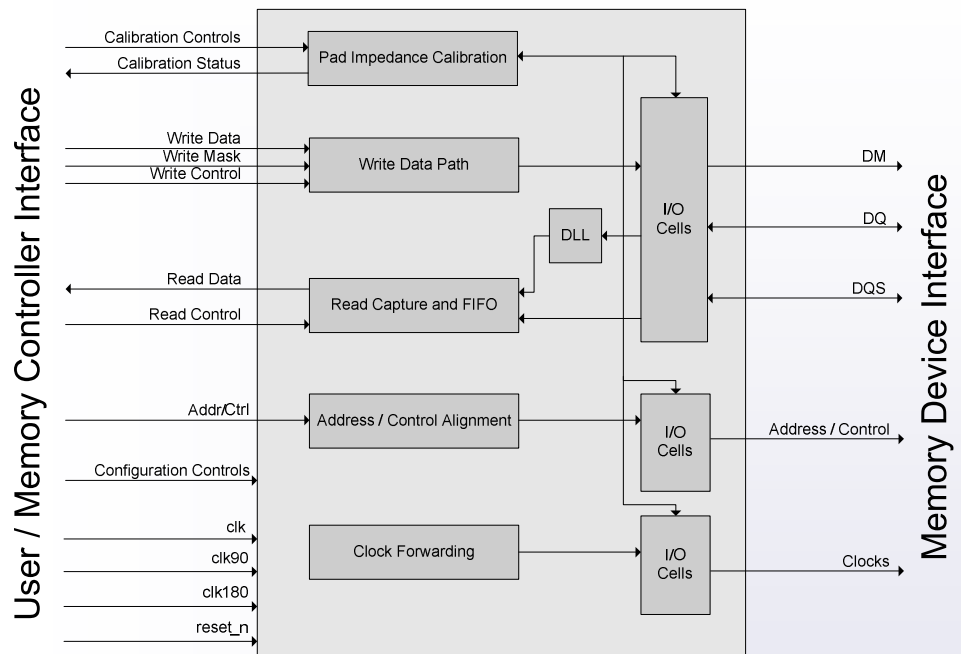


## Product Highlights

- Silicon-proven DDR PHY for use in eASIC NX devices
- Supports DDR2 SDRAM 533, DDR SDRAM 400, Mobile DDR SDRAM 400 Mbit/s/pin operation
- Uses robust windowing data capture method
- Uses internal eASIC DDR I/O and DLL
- Supports ASIC-side ODT
- Supports Byte and Nibble DQS
- Supports a broad range of programmable features including timing, termination, drive strengths, etc.
- Calibrated output and termination impedance
- Comprehensive memory test support
- Provided as a soft core with timing constraints enabling optimization for a target pinout
- Customization and Integration services available

## Block Diagram



## Product Overview

The combination of Northwest Logic's Memory Controller Cores and ASIC DDR PHY is designed for use in eASICs NX devices requiring high memory throughput, high clock rates and full programmability.

Versions of the eASIC DDR PHY are available which support DDR2 SDRAM 533, DDR SDRAM 400, and Mobile DDR SDRAM 400 SDRAM Mbit/s/pin operation.

To ensure robust operation the DDR PHY uses a windowing data capture method, uses internal eASIC DDR I/O and DLL, and supports ASIC-side ODT and calibrated output impedance.

The DDR PHY is specifically designed for flexibility. This includes a broad range of programmable features including various timing parameters, termination settings and drive strengths.

The combination of the Memory Controller Core and DDR PHY can be fully tested using Northwest Logic's Memory Test Core and Data Analyzer Core. The Memory Test Core provides a complete memory test using random and directed reads and writes. The Data Analyzer Core provides access to the actual

and expected memory test results for analysis.

The DDR PHY is delivered as a soft core with timing constraints. This enables the DDR PHY to be optimized for a target pinout.

Northwest Logic can provide DDR PHY related services including DDR PHY hardening. Contact Northwest Logic for a quote.

### Product Deliverables:

- Core (Netlist or Source Code)
- Timing constraints
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates