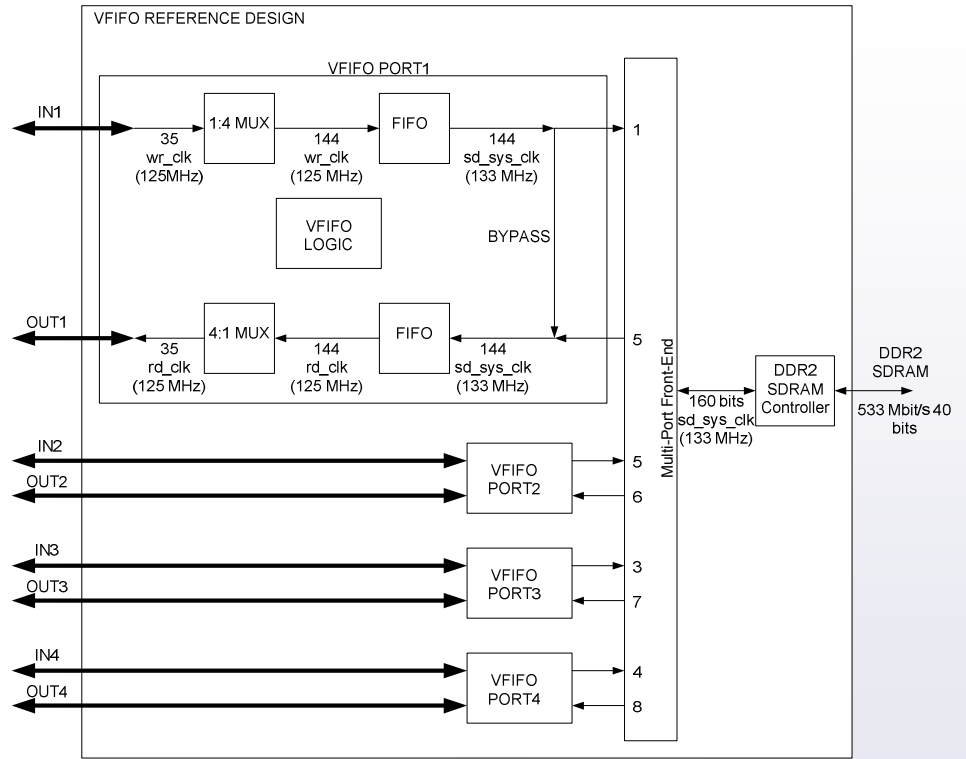


Product Highlights

- Converts a segment of memory into a Virtual FIFO (VFIFO)
- Can be used in single port or multi port configurations
- Bypass mode eliminates input to output port latency when memory is empty
- Supports full rate and half rate Memory Controller Core operation
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Virtual FIFO (VFIFO) Core converts a segment of memory into a virtual FIFO.

The core consists of an input port and an output port. User logic writes data into the input port and reads it from the output port. The core strives to always keep the input port empty so that it can accept user data and the output port full so that it can provide user data.

To minimize latency, data automatically flows from the input port to the output port bypassing the external memory until the output port fills up. At that point in time, data will start flowing through the memory controller and into the external memory. This continues until the external memory has been emptied enabling the VFIFO Core to switch back to bypass mode.

The core is attached to two ports of Northwest Logic's Multi-Port Front-End Core. Consequently, multiple virtual FIFO can be created by using multiple instances of the VFIFO core with the Multi-Port Front-End Core.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates