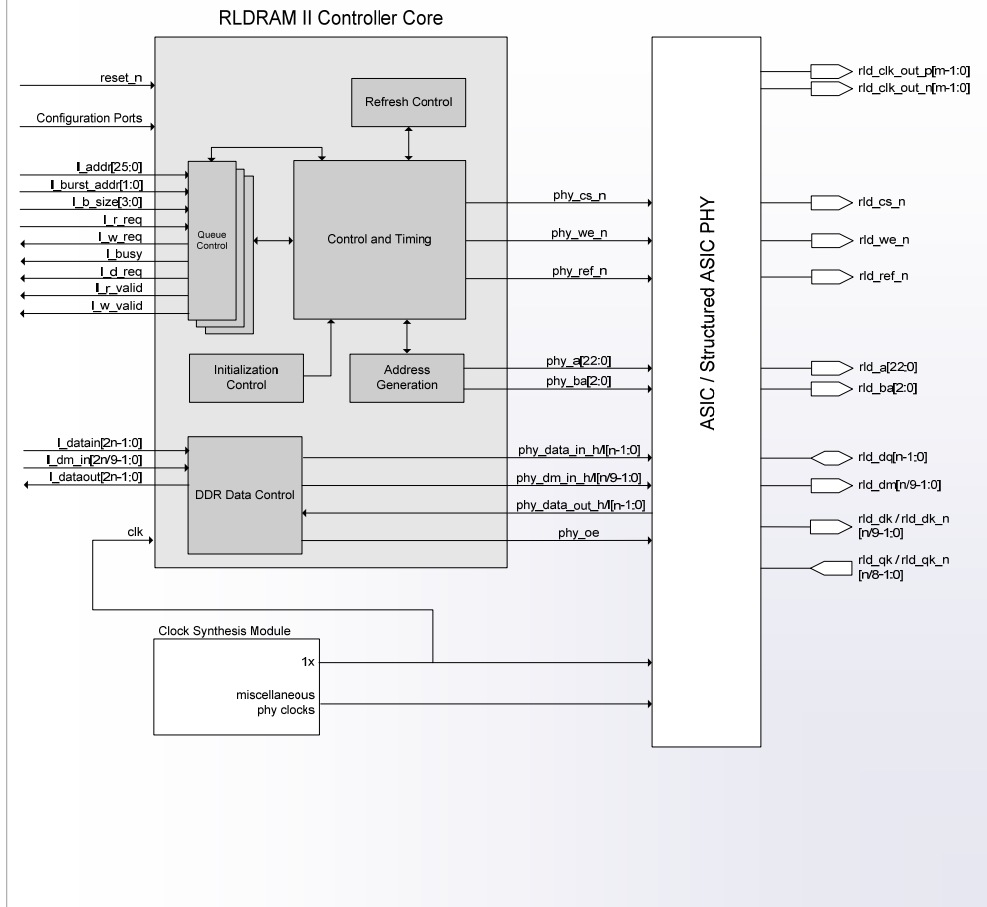


Product Highlights

- Maximizes bus efficiency via command queuing
- Minimal latency achieved via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Supports full rate and half-rate clock operation
- Full run-time configurable timing parameters and memory settings
- Full set of Add-On Cores and ASIC DDR PHY available
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Reduced Latency DRAM (RLDRAM) II Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core has been optimized to take advantage of the fast random cycle and fast access times available with RLDRAM II. The core also supports both common and separate data buses and multiplexed and non-multiplexed addressing.

The core accepts commands using a simple local interface and translates them to the command sequences required by RLDRAM II devices. The core also performs all initialization and refresh functions.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all RLDRAM II configurations.

Northwest Logic offers a full set of Add-Cores and an ASIC DDR PHY for use with the core.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates