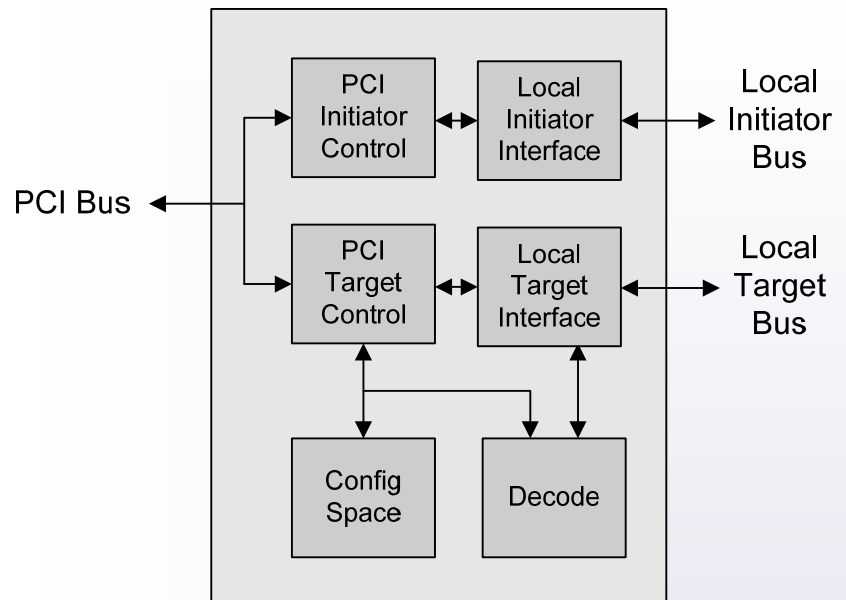


## Product Highlights

- High-performance, easy-to-use core
- Achieves push-button timing with minimal routing constraints
- Minimal size
- Supports 33/66 MHz, 32/64 bit operation
- Master/Target and Target-Only versions available
- Host and Peripheral versions available
- User expandable configuration space can be loaded from EEPROM
- Provided with a comprehensive Verification Suite
- Works with DMA Back-End Core and DMA Driver
- PCI Local Bus Specification Revision 3.0 compliant
- Source code available
- Customization and Integration services available

## Block Diagram



## Product Overview

Northwest Logic's PCI Core has been specifically designed to be easy-to-use:

- Hides the complexities and timing issues of the PCI Bus from the user
- Control interface has consistent timing and function over all modes of operation
- Data interface connects directly to FIFOs
- Provides complete error-handling support
- Achieves push-button timing with minimal routing constraints

The PCI Core implements the "front-end" of a PCI design giving the user complete control of the "back-end" functionality. This flexibility is further enhanced with a user expandable configuration space. This PCI Core supports automatic loading of the configuration space via a EEPROM.

The core also integrates with the DMA Back-End Core and DMA Driver to provide a complete DMA solution.

The core is available in several flavors including 32 vs. 64 bit, Target-Only vs. Master/Target, and Peripheral vs. Host.

The core is provided with the PCI-X/PCI Verification Suite which provides complete scripting and random stimulus capabilities enabling the user design to be fully validated prior to use in hardware.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

### Product Deliverables:

- Core (Netlist or Source Code)
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates