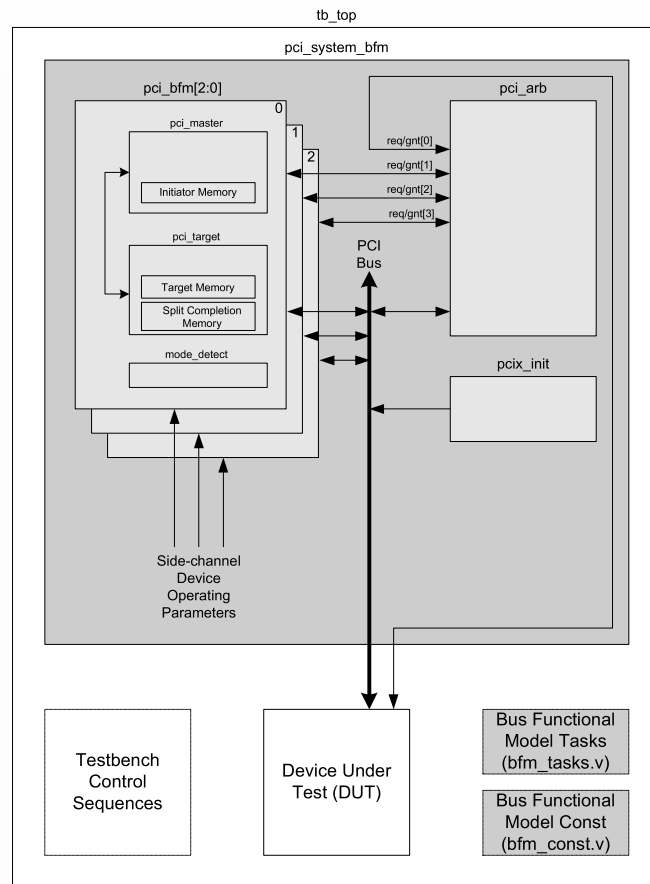


## Product Highlights

- Complete verification environment for PCI-X / PCI designs
- Models all PCI-X and PCI bus behaviors
- Dynamically programmable probabilities for all flow control signaling (master/target wait states, retries, disconnects, split responses, etc.)
- Includes models for master and target behaviors and fully compliant PCI-X / PCI bus arbiter
- Includes rich set of high-level tasks calls for initiating various forms of bus traffic including host configuration and test pattern generation
- Provided with an extensive set of example testbench control sequences
- PCI Local Bus Specification Revision 3.0 and PCI-X Local Bus Specification Revision 2.0 (Mode 1) compliant
- Provided in clear text source

## Block Diagram



## Product Overview

Northwest Logic's PCI-X / PCI Verification Suite is a full featured environment for verification of a PCI-X or PCI design.

The standard environment includes three instances of device bus functional models, enabling simulation of multi-device, high traffic conditions. The environment also includes a fully compliant PCI-X / PCI arbiter and bus mode detection circuits.

High level task calls are provided to enable easy generation and of complex bus traffic with regressive checking of data integrity. Tasks are also included which perform complete host configuration of all devices on primary and secondary busses.

Each bus functional model instance contains parameterized memory for master and target side transactions. Additionally memory is provided for up to 32 tags of split completions. The initiator model automatically transfers data between target and master memory for split completions.

Each bus functional model is programmed with probabilities for modeling various target behaviors including target wait states, retries, disconnects, split responses, and 64/32-bit transaction

conversion. Each bus functional model can be independently programmed for any decode speed.

An extensive set of testbench control sequences are provided, demonstrating initiation of transactions and control of bus functional model target behavior.

The Verification Suite is fully compliant with PCI Local Bus Specification Revision 3.0 and PCI-X Local Bus Specification Revision 2.0 (Mode 1).

### Verification Suite Deliverables:

- Verification Suite (Source Code)
- Documentation
- Expert Technical Support & Maintenance Updates