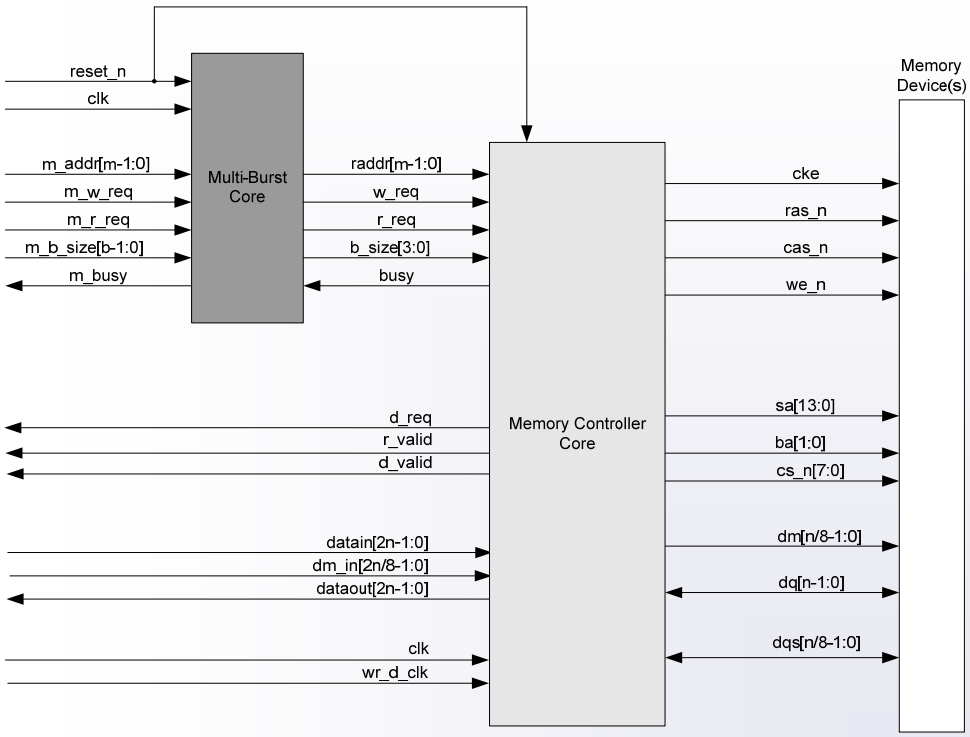
Multi-Burst Core

Product Highlights

- Automatically breaks long burst requests into multiple requests matching the memory's native burst length
- Automatically partitions requests that are not aligned on a boundary of the memory's native burst length into multiple requests
- Simple user interface signaling (identical to Northwest Logic Memory Controller Cores)
- Included with Multi-Port Front-End Core and Read-Modify-Write Core
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

The Multi-Burst Core automatically breaks long burst requests into multiple requests matching the memory's native burst length. This enables read or write requests of 256 data cycles or more.

The core also automatically partitions requests that are not aligned on a boundary of the memory's native burst length into multiple requests.

The core provides a simple user interface which is identical to standard Northwest Logic's Memory Controller Cores Local Interface. The maximum request size is typically configured for 256 data cycles. However, this can be configured to larger values at the expense of routing delay and resource usage.

Northwest Logic delivers the core integrated with the target Memory Controller Core. The Multi-Burst Core is included with the Multi-Port Front-End Core and Read-Modify-Write Cores.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates

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