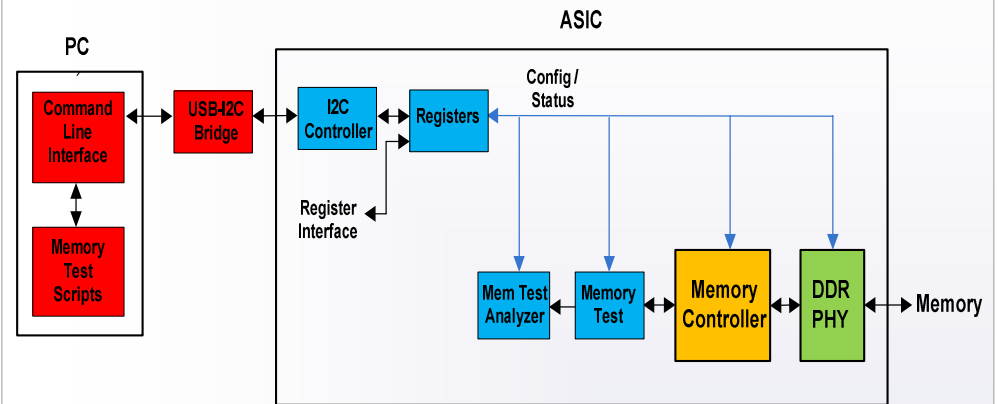


Product Highlights

- Part of Northwest Logic's comprehensive Memory Test Package
- Provides a complete random address and data memory test
- Supports walking ones and zeros, counting and arbitrary (user programmable) data patterns
- Supports sequential, random and arbitrary (user programmable) address patterns
- Useful for chip and board validation
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

The Memory Test Core provides a random data and address memory test.

The core supports walking ones and zeroes, counting, random, and arbitrary (user programmable) data patterns. The core also supports sequential, random and arbitrary (user programmable) address patterns.

The core is useful for chip and board validation. The pseudo-random data pattern is particularly useful because it can fully stress both the chip and board design.

The Mem Test Analyzer Core can be used in conjunction with the Memory Test Core to capture the actual and expected test data. The capture is initiated by an error trigger signal provided by the Memory Test Core. This data can then be retrieved from the Mem Test Analyzer Core via the chip's configuration & status bus, on-chip processor or dedicated low-pin count serial port.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates