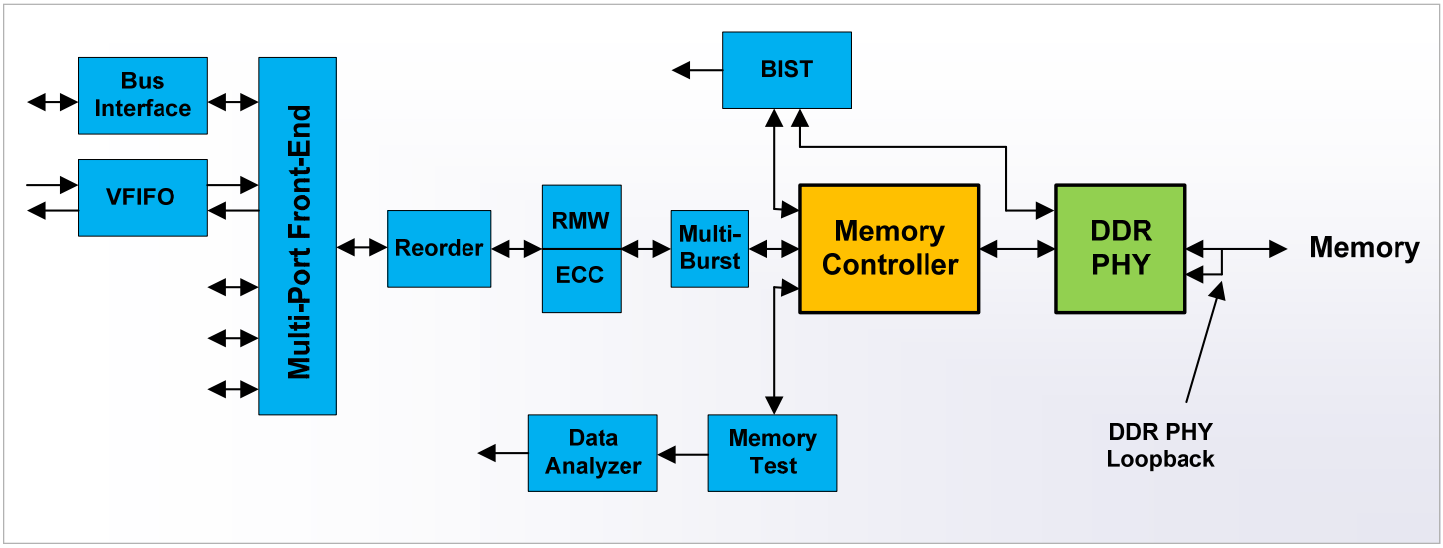
Memory Interface Solution



Solution Includes:

Add-On Cores

- Bus Interface Cores
  - Support AHB, AXI, Avalon, PLB buses
- VFIFO Core
  - Turns a segment of memory into a Virtual FIFO
- Multi-Port Front-End Core
  - Provides fully arbitrated, multi-port interface
- Reorder Core
  - Provides data coherent request reordering based on priority and optimal bus utilization
- Read-Modify-Write (RMW) Core
  - Handles writing non-aligned bursts into ECC protected memory
- Error Correcting Code (ECC) Core
  - Provides standard DRAM error detection / correction
- Multi-Burst Core
  - Breaks extended bursts into multiple native memory bursts
- Memory Test Core
  - Performs a random data and address memory test
- Data Analyzer Core
  - Used to capture on-chip signals of interest
- BIST Core
  - Provides at-speed Memory Controller Core + DDR PHY production test

Memory Controller Cores

- Support broad variety of DRAMs including DDR3/DDR2/DDR/SDR SDRAM, Mobile DDR/SDR SDRAM and RLDRAM II

DDR PHY

- Provides a complete DRAM physical interface
- Integrates third party DDR I/O and DLL

Key Features:

- Complete solution handling all design, test and bring-up challenges
- Fully silicon validated
- Supports full range of memory configurations (on-board chips, single DIMM, multiple DIMMs, etc.)
- Provides high bus efficiency
- Minimal latency achieved via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Can be flexibly configured for target application
- Simple, easy-to-use interfaces
- Full run-time configurable timing parameters and memory settings
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Provided with expert technical support
- IP Customization and Logic, Board, and Software Development services available