



Solution Includes:

Add-On Cores

- Support AXI, AHB, PLB Interfaces
- Multi-port, QOS-based arbitration support
- Efficiency-based reordering maximizes memory utilization
- Read-Modify-Write and ECC support
- Comprehensive Memory Test Package enables easy chip and board bring-up

Memory Controller Cores

- Supports DDR3/DDR2/DDR/SDR SDRAM, Mobile DDR/SDR SDRAM and RLDRAM II
- Supports DDR3/2 (2133/1066) operation
- 32 bank and 8 deep command queue support
- Supports Full Rate and Half Rate operation for FPGA prototyping

DDR PHY

- Fully integrated with a broad variety of third-party PHYs
- Offer silicon-proven Northwest Logic soft PHY

Key Features:

- Complete solution handling all design, test and bring-up challenges
- Fully silicon validated
- Supports full range of memory configurations (on-board chips, single DIMM, multiple DIMMs, etc.)
- Provides high memory efficiency with minimal latency
- Minimal latency achieved via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Can be flexibly configured for target application
- Simple, easy-to-use interfaces
- Full run-time configurable timing parameters and memory settings
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Provided with expert technical support
- IP Customization and Logic, Board, and Software Development services available