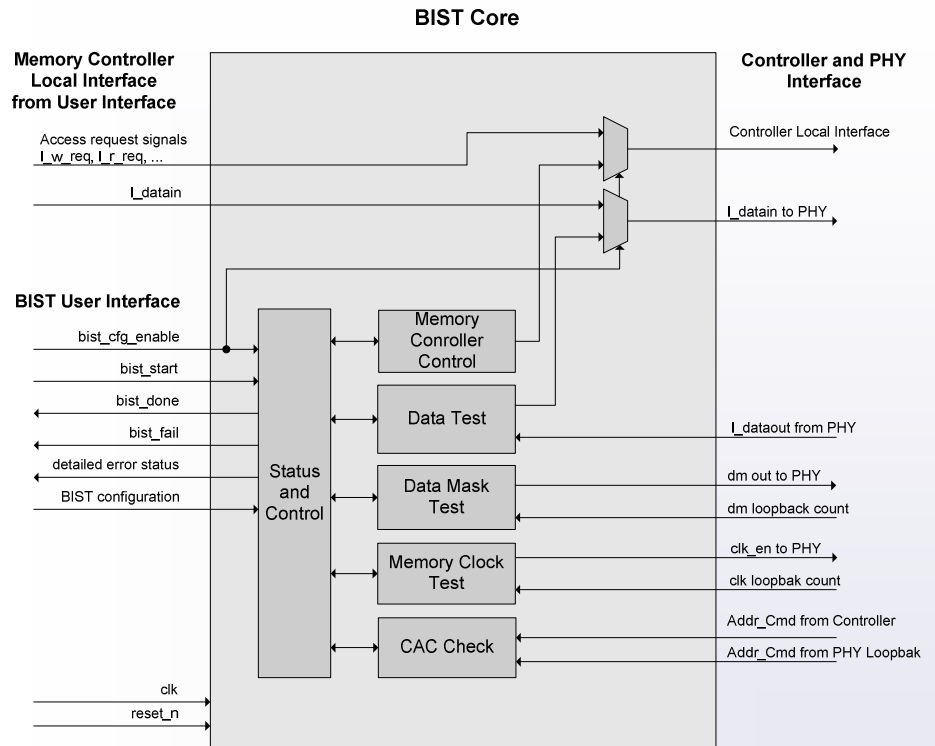


## Product Highlights

- Provides an at-speed DDR PHY test
- Test is conducted while the DDR PHY is in loopback eliminating the connection to external memory
- Includes Data, Command-Address-Control (CAC), Memory Clock and Data Mask loopback tests
- Useful for chip production and bring-up testing
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

## Block Diagram



## Product Overview

The Built-In-Self-Test (BIST) Core provides an at-speed test of the DDR PHY.

The core performs the test while the DDR PHY is in loopback eliminating the connection to external memory. This enables the test to be performed as part of the chip production testing. The test is also useful during chip and board bring-up.

The test includes Data, Command-Address-Control (CAC), Memory Clock and Data Mask loopback tests. The tests are run in parallel to minimize test time.

The BIST test returns a pass/no pass result. This test result is typically accessed via the chip's configuration and status bus.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

### Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates